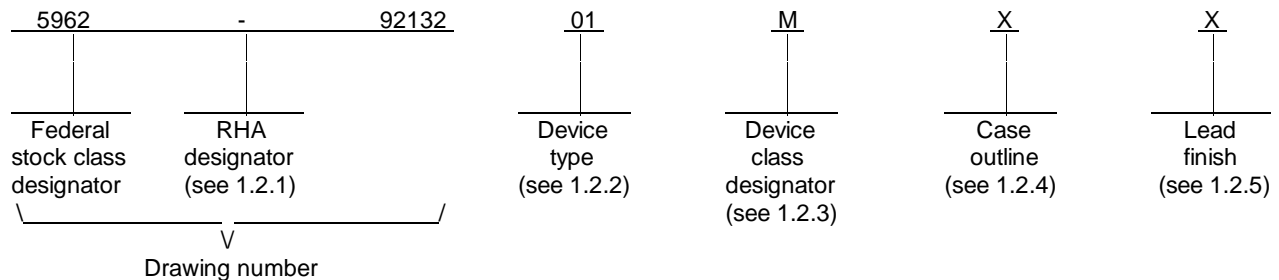


[illegible]

## 1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Refresh
01	4C4067	64K x 4 bit DRAM	100 ns	256 cycles (4 ms)
02	4C4067	64K x 4 bit DRAM	120 ns	256 cycles (4 ms)
03	4C4067	64K x 4 bit DRAM	150 ns	256 cycles (4 ms)

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18	18	Dual-in-line
X	See figure 1	18	Leadless chip carrier
Y	See figure 1	18	Leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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### 1.3 Absolute maximum ratings. 1/

Voltage on any pin relative to $V_{SS}$ .....	-1.5 V to +7.0 V
Short-circuit output current .....	50 mA
Power dissipation ( $P_D$ ) .....	1.0 W
Storage temperature range .....	-65° C to +150° C
Lead temperature (soldering, 5 seconds) .....	+300° C
Thermal resistance ( $\theta_{JC}$ ):	
Case V .....	See MIL-STD-1835
Cases X and Y .....	50° C/W
Junction temperature ( $T_J$ ) .....	+150° C

### 1.4 Recommended operating conditions.

Supply voltage ( $V_{CC}$ ) .....	4.5 V dc to 5.5 V dc
Power supply and signal reference ( $V_{SS}$ ) .....	0.0 V dc
High level input voltage ( $V_{IH}$ ) .....	2.4 V dc to 6.5 V dc
Low level input voltage ( $V_{IL}$ ) .....	-1.0 V dc to +0.8 V dc
Case operating temperature ( $T_C$ ) .....	-55° C to +125° C
Refresh cycle time .....	4.0 ms

### 1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) .....	2/ percent
---	------------

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

### STANDARDS

#### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-973 - Configuration Management.  
MIL-STD-1835 - Microcircuit Case Outlines.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

### HANDBOOK

#### MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Values will be added when they become available.

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(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-I-38535, appendix A).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
  - (1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage 5/	V <sub>OH</sub>	V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -5 mA, V <sub>IH</sub> = 2.4 V	1, 2, 3	All	2.4		V
Low level output voltage 5/	V <sub>OL</sub>	V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = 5 mA, V <sub>IH</sub> = 2.4 V	1, 2, 3	All		0.4	
High level input leakage current	I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 6.5 V	1, 2, 3	All		10	μA
Low level input leakage current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.0 V	1, 2, 3	All		-10	
High level output leakage current	I <sub>OH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 6.5 V	1, 2, 3	All		10	
Low level output leakage current	I <sub>OL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.0 V	1, 2, 3	All		-10	
Average operating current during READ 6/ or WRITE cycle	I <sub>CC1</sub>	T <sub>C</sub> = minimum cycle	1, 2, 3	All		60	mA
Average page-mode current 6/	I <sub>CC2</sub>	T <sub>C</sub> (P) = minimum cycle, RAS low, CAS cycling	1, 2, 3	All		55	
Standby current	I <sub>CC3</sub>	After 1 memory cycle RAS and CAS high	1, 2, 3	All		8	
Average refresh current (RAS only REFRESH) 6/	I <sub>CC4</sub>	T <sub>C</sub> = minimum cycle, CAS high, RAS cycling	1, 2, 3	All		60	
Standby current (CAS before RAS refresh) 7/	I <sub>CC5</sub>	T <sub>C</sub> (P) = minimum cycle, RAS and CAS cycling	1, 2, 3	All		60	
Input capacitance, A <sub>0</sub> - A <sub>7</sub> , D <sub>IN</sub> 7/	C <sub>I1</sub>	T <sub>C</sub> = +25°C, f = 1 MHz See 4.4.1e	4	All		6	pF
Input capacitance, RAS, CAS, WE, OE 7/	C <sub>I2</sub>	T <sub>C</sub> = +25°C, f = 1 MHz See 4.4.1e	4	All		8	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance, D <sub>OUT</sub> 7/	C <sub>O</sub>	T <sub>C</sub> = +25°C, f = 1 MHz See 4.4.1e	4	All		8	pF
Functional test		See 4.4.1c	7, 8A, 8B	All			
Access time from RAS 8/	t <sub>a(R)</sub>	See figures 4 and 5	9, 10, 11	01		100	ns
				02		120	
				03		150	
Access time from CAS 9/	t <sub>a(C)</sub>		9, 10, 11	01		50	
				02		60	
				03		75	
Output disable time after CAS high 10/	t <sub>dis(CH)</sub>		9, 10, 11	All		40	
Page-mode cycle time 11/	t <sub>c(P)</sub>		9, 10, 11	01	90		
				02	100		
				03	120		
Read cycle time	t <sub>c(rd)</sub>		9, 10, 11	01	195		
				02	220		
				03	250		
Write cycle time	t <sub>c(W)</sub>		9, 10, 11	01	195		
				02	220		
				03	250		
Read-write/read-modify- write cycle time 11/	t <sub>c(rdW)</sub>		9, 10, 11	01	250		
				02	290		
				03	315		
Pulse duration, CAS high (page mode)	t <sub>W(CH)P</sub>		9, 10, 11	01, 02	30		
				03	35		
Pulse duration, CAS low	t <sub>W(CL)</sub>		9, 10, 11	01	50	1000	
				02	60	1000	
				03	75	1000	
Pulse duration, RAS high (precharge time) 12/ (page mode)	t <sub>W(RH)P</sub>		9, 10, 11	01, 02	80		
				03	90		
Pulse duration, RAS high (precharge time) (non-page mode)	t <sub>W(RH)</sub>		9, 10, 11	01, 02	80		
				03	90		
Pulse duration, RAS low	t <sub>W(RL)</sub>		9, 10, 11	01	100	1000	
				02	120	1000	
				03	150	1000	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> <u>3/</u> <u>4/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write pulse duration	t <sub>w(W)</sub>	See figures 4 and 5	9, 10, 11	01	35		ns
				02	40		
				03	45		
Column address setup time <u>11/</u>	t <sub>su(CA)</sub>		9, 10, 11	All	0		
Row address setup time <u>11/</u>	t <sub>su(RA)</sub>		9, 10, 11	All	0		
Data setup time <u>11/</u> <u>13/</u>	t <sub>su(D)</sub>		9, 10, 11	All	0		
Read command setup time <u>11/</u>	t <sub>su(rd)</sub>		9, 10, 11	All	0		
Early write command setup time before CAS low <u>14/</u>	t <sub>su(WCL)</sub>		9, 10, 11	All	0		
Write command setup time before CAS high	t <sub>su(WCH)</sub>		9, 10, 11	01	35		
				02	40		
				03	45		
Write command setup time before RAS high	t <sub>su(WRH)</sub>		9, 10, 11	01	35		
				02	40		
				03	45		
Column address hold time after CAS low	t <sub>h(CLCA)</sub>		9, 10, 11	01	20		
				02, 03	30		
Row address hold time	t <sub>h(RA)</sub>		9, 10, 11	01	15		
				02, 03	20		
Column address hold time after RAS low	t <sub>h(RLCA)</sub> t <sub>su(RLCA)</sub>		9, 10, 11	01	70		
				02	80		
				03	100		
Data hold time after CAS low <u>13/</u>	t <sub>h(CLD)</sub>		9, 10, 11	01, 02	35		
				03	45		
Data hold time after RAS low	t <sub>h(RLD)</sub>		9, 10, 11	01	85		
				02	100		
				03	120		
RAS before CAS precharge <u>11/</u>	t <sub>RHCL</sub>		9, 10, 11	All	0		

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> <u>3/</u> <u>4/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time after W low <u>13/</u>	t <sub>h(WLD)</sub>	See figures 4 and 5	9, 10, 11	01, 02	35		ns
				03	45		
Read command hold time after CAS high <u>11/</u>	t <sub>h(CHrd)</sub>		9, 10, 11	All	0		
Read command hold time after RAS high <u>11/</u>	t <sub>h(RHrd)</sub>		9, 10, 11	All	10		
Write command hold time after CAS low	t <sub>h(CLW)</sub>		9, 10, 11	01	35		
				02	40		
				03	45		
Write command hold time after RAS low	t <sub>h(RLW)</sub>		9, 10, 11	01	85		
				02	100		
				03	120		
Delay time, RAS low to CAS high	t <sub>RLCH)</sub>		9, 10, 11	01	110		
				02	120		
				03	150		
Delay time, CAS high to RAS low	t <sub>CHRL</sub>		9, 10, 11	All	5		
Delay time, CAS low to RAS high	t <sub>CLR H</sub>		9, 10, 11	01	50		
				02	60		
				03	75		
Delay time, RAS low to CAS high (CAS before RAS refresh only)	t <sub>RLCHR</sub>		9, 10, 11	01	20		
				02	25		
				03	30		
Delay time, CAS low to RAS low (CAS before RAS refresh only) <u>15/</u>	t <sub>CLRL</sub>	9, 10, 11	All	10			
Delay time, CAS low to W low (read-modify-write cycle only) <u>14/</u> <u>16/</u>	t <sub>CLWL</sub>	9, 10, 11	01	30			
			02	50			
			03	60			
Delay time, RAS low to CAS low	t <sub>RLCL</sub>	9, 10, 11	01	25	50		
			02	30	60		
			03	30	75		
Delay time, RAS low to W low (read-modify-write cycle only) <u>14/</u> <u>16/</u>	t <sub>RLWL</sub>	9, 10, 11	01	80			
			20	110			
			03	135			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> <u>3/</u> <u>4/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Refresh time interval <u>17/</u> <u>18/</u>	t <sub>rf</sub>	See figures 4 and 5	9, 10, 11	All		4.0	ms
Transition time (rise and fall)	t <sub>t</sub>		9, 10, 11	All	3	100	ns
Output disable time after OE high	t <sub>dis</sub> (GH)		9, 10, 11	01		35	
				02, 03		40	
Output enable time after OE low <u>19/</u>	t <sub>en</sub> (GL)		9, 10, 11	01, 02		25	
				03		30	

- 1/ An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (READ, WRITE, READ-MODIFY-WRITE, RAS refresh) before proper device operation is assured.
- 2/ AC characteristics assume transition time (t<sub>r</sub>) = 5 ns. Input levels are from GND to 3.0 V. Input and output timing reference levels are 1.5 V.
- 3/ V<sub>IL</sub> (max) and V<sub>IH</sub> (min) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IL</sub> and V<sub>IH</sub>.
- 4/ In addition to meeting the transition rate specification, all input signals must make the transition between V<sub>IL</sub> and V<sub>IH</sub> (or V<sub>IH</sub> and V<sub>IL</sub>) in a monotonic manner.
- 5/ V<sub>SS</sub> is common for all voltages.
- 6/ Specified values are obtained with the output load equal to 2 TTL loads and 100 pF to V<sub>SS</sub>.
- 7/ Capacitance measured with a Boonton meter or equivalent or effective capacitance calculated from the equation C=IΔt/ΔV with ΔV equal to 3 volts and V<sub>CC</sub> equal to 5.0 V. Capacitance shall be measured only for the initial qualification and after process or design changes which may effect terminal capacitance.
- 8/ Assumes that t<sub>RLCL</sub> < (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>a(R)</sub> will increase by the amount that t<sub>RLCL</sub> exceeds the value shown.
- 9/ Assumes that t<sub>RLCL</sub> ≥ t<sub>RLCL</sub> (max).
- 10/ t<sub>dis</sub>(CH) (max) defines the time at which the output achieves the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
- 11/ Some parameters are conditionally guaranteed that are specified to aid device application. They are not necessarily directly verified by a specific test, however, the vendor uses device characterizations and design specifications to insure all device parameters are within specified performance limits.
- 12/ If CAS is low at the falling edge of RAS, D<sub>OUT</sub> will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for t<sub>c(P)</sub>. Footnote 20/ applies to determine valid data out.
- 13/ These parameters are referenced to CAS leading edge in early WRITE cycles and to WE leading edge in late WRITE or READ-MODIFY-WRITE cycles.
- 14/ t<sub>su</sub>(WCL), t<sub>CLWL</sub> and t<sub>RLWL</sub> are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If t<sub>su</sub>(WCL) ≥ t<sub>su</sub>(WCL) (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If t<sub>CLWL</sub> ≥ t<sub>CLWL</sub> (min) and t<sub>RLWL</sub> ≥ t<sub>RLWL</sub> (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until CAS goes back to V<sub>IH</sub>) is indeterminate.
- 15/ Enables on-chip refresh and address counters.
- 16/ During a READ-WRITE or READ-MODIFY-WRITE cycle the minimum specifications for t<sub>RWD</sub> and t<sub>CWD</sub> must be modified by adding 40 ns to each specification due to OE delay.
- 17/ A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625 μs so that all 256 RAS address combinations are executed within 4 ms (regardless of sequence). Distributed refresh is recommended.
- 18/ A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of RAS addresses (regardless of sequence). This refresh mode must be executed within 4 ms.
- 19/ If OE is taken low then high (V<sub>IH</sub>) D<sub>OUT</sub> goes open. If OE is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.
- 20/ If CAS = V<sub>IH</sub> or OE = V<sub>IH</sub> data output is high impedance. If CAS = V<sub>IL</sub> and OE = V<sub>IL</sub> data output may contain data from the last valid READ cycle.

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# Case X

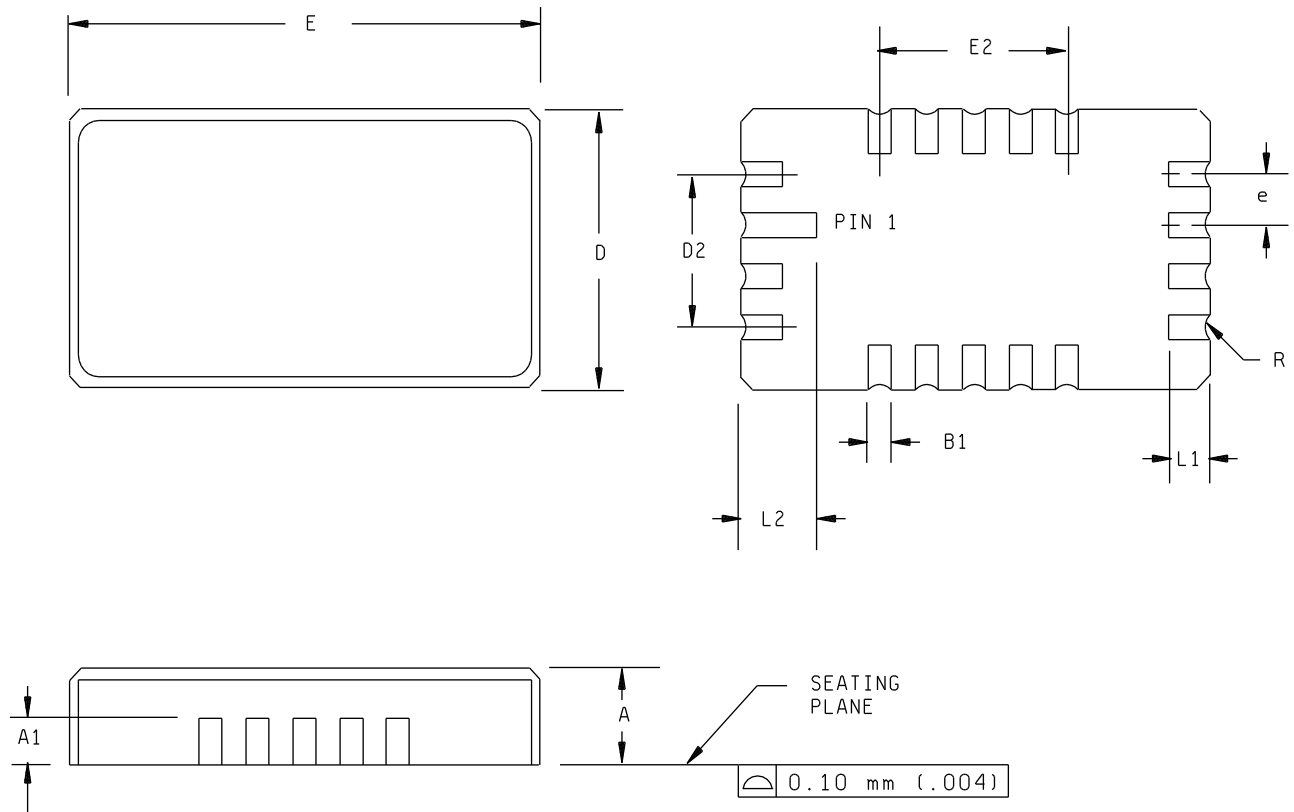


FIGURE 1. Case outline.

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Symbol	Dimensions shown in			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.40	1.91	.055	.075
A <sub>1</sub>	0.89	1.14	.035	.045
B <sub>1</sub>	0.56	0.71	.022	.028
D	7.11	7.49	.280	.295
D <sub>2</sub>	3.81 REF		.150 REF	
E	12.32	12.83	.485	.505
E <sub>2</sub>	5.08 REF		.200 REF	
e	1.27 BSC		.050 BSC	
L <sub>1</sub>	1.14	1.40	.045	.055
L <sub>2</sub>	1.91	2.31	.075	.091
N	18		18	
R	0.10 R	0.36 R	.004 R	.014 R
ND	4		4	
NE	5		5	

Note: The U.S. government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

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# Case Y

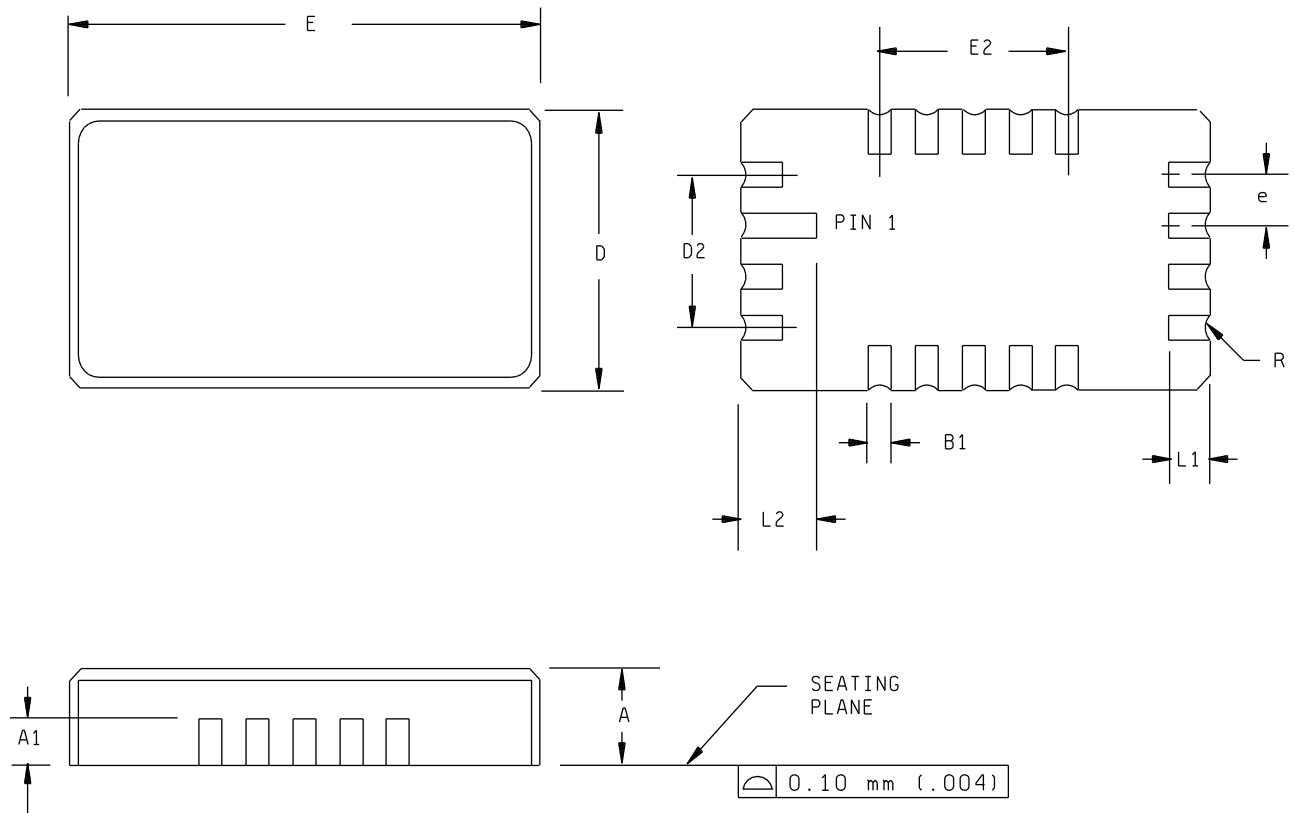


FIGURE 1. Case outline - Continued.

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Symbol	Dimensions shown in			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.47	1.83	.058	.072
A <sub>1</sub>	1.14	1.40	.045	.055
B <sub>1</sub>	0.15	0.56	.006	.022
D	7.11	7.37	.280	.290
D <sub>2</sub>	3.81 REF		.150 REF	
E	11.28	11.58	.444	.456
E <sub>2</sub>	5.08 REF		.200 REF	
e	1.27 BSC		.050 BSC	
L <sub>1</sub>	1.14	1.40	.045	.055
L <sub>2</sub>	1.96	2.36	.077	.093
N	18		18	
R	0.10 R	0.36 R	.004 R	.014 R
ND	4		4	
NE	5		5	

Note: The U.S. government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

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Device types	All
Case outlines	V, X, Y
Terminal number	Terminal symbol
1	$\overline{\text{OE}}$
2	$\text{I/O}_1$
3	$\text{I/O}_2$
4	$\overline{\text{WE}}$
5	$\overline{\text{RAS}}$
6	$\text{A}_6$
7	$\text{A}_5$
8	$\text{A}_4$
9	$\text{V}_{\text{CC}}$
10	$\text{A}_7$
11	$\text{A}_3$
12	$\text{A}_2$
13	$\text{A}_1$
14	$\text{A}_0$
15	$\text{I/O}_3$
16	$\overline{\text{CAS}}$
17	$\text{I/O}_4$
18	$\text{V}_{\text{SS}}$

FIGURE 2. Terminal connections.

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Operation	Inputs						Input/Output
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row address	Column address	
Standby	H	H	H	H	X	X	High-Z
Read	L	L	L	X	Row	Col	Data out
Write (early write)	L	L	L	X	Row	Col	Data in
Read-write	L	L	H $\rightarrow$ L $\rightarrow$ H	L $\rightarrow$ H	Row	Col	Data out, Data in
Page-mode read	L	H $\rightarrow$ L $\rightarrow$ H	H	L	Row	Col	Data out, Data out
Page-mode write	L	H $\rightarrow$ L $\rightarrow$ H	L	X	Row	Col	Data in, Data in
Page-mode read-write	L	H $\rightarrow$ L $\rightarrow$ H	H $\rightarrow$ L $\rightarrow$ H	L $\rightarrow$ H	Row	Col	Data out, Data in
$\overline{\text{RAS}}$ -only refresh	L	H	X	H	Row	N/A	High-Z
Hidden refresh	L $\rightarrow$ H $\rightarrow$ L	L	H	L	Row	Col	Data out
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	H $\rightarrow$ L	L	X	X	X	X	High-Z

X = Don't care

FIGURE 3. Truth table.

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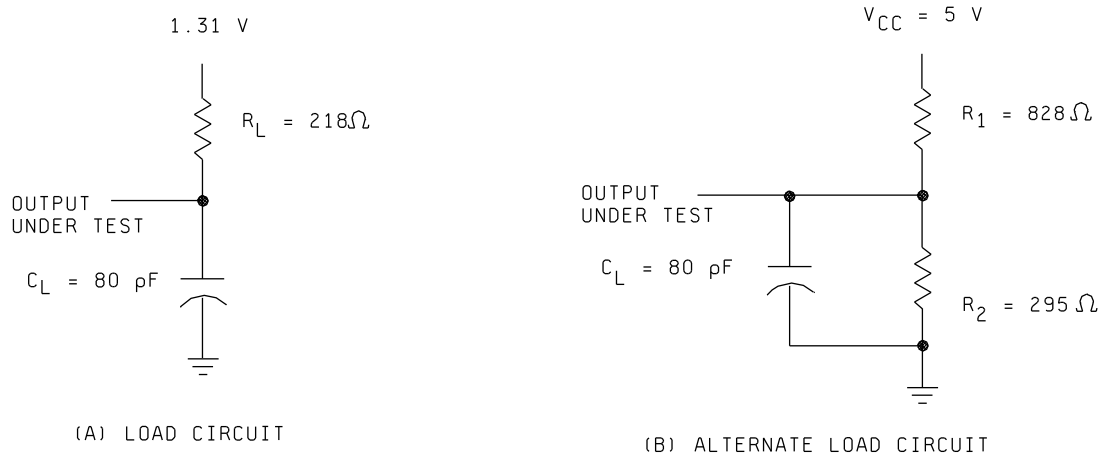


FIGURE 4. Load circuit.

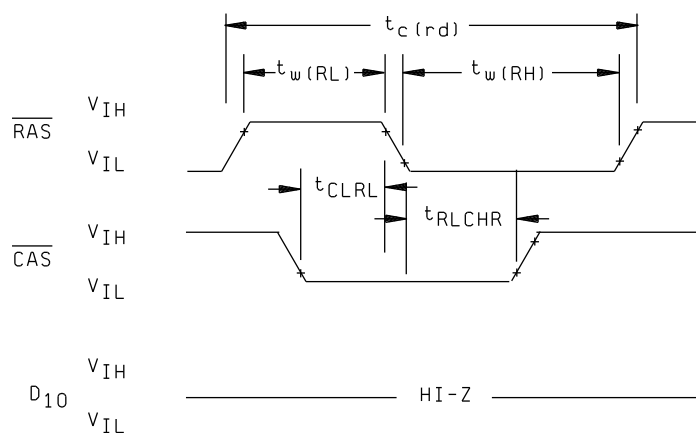


FIGURE 5. Switching waveforms.

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# Read cycle

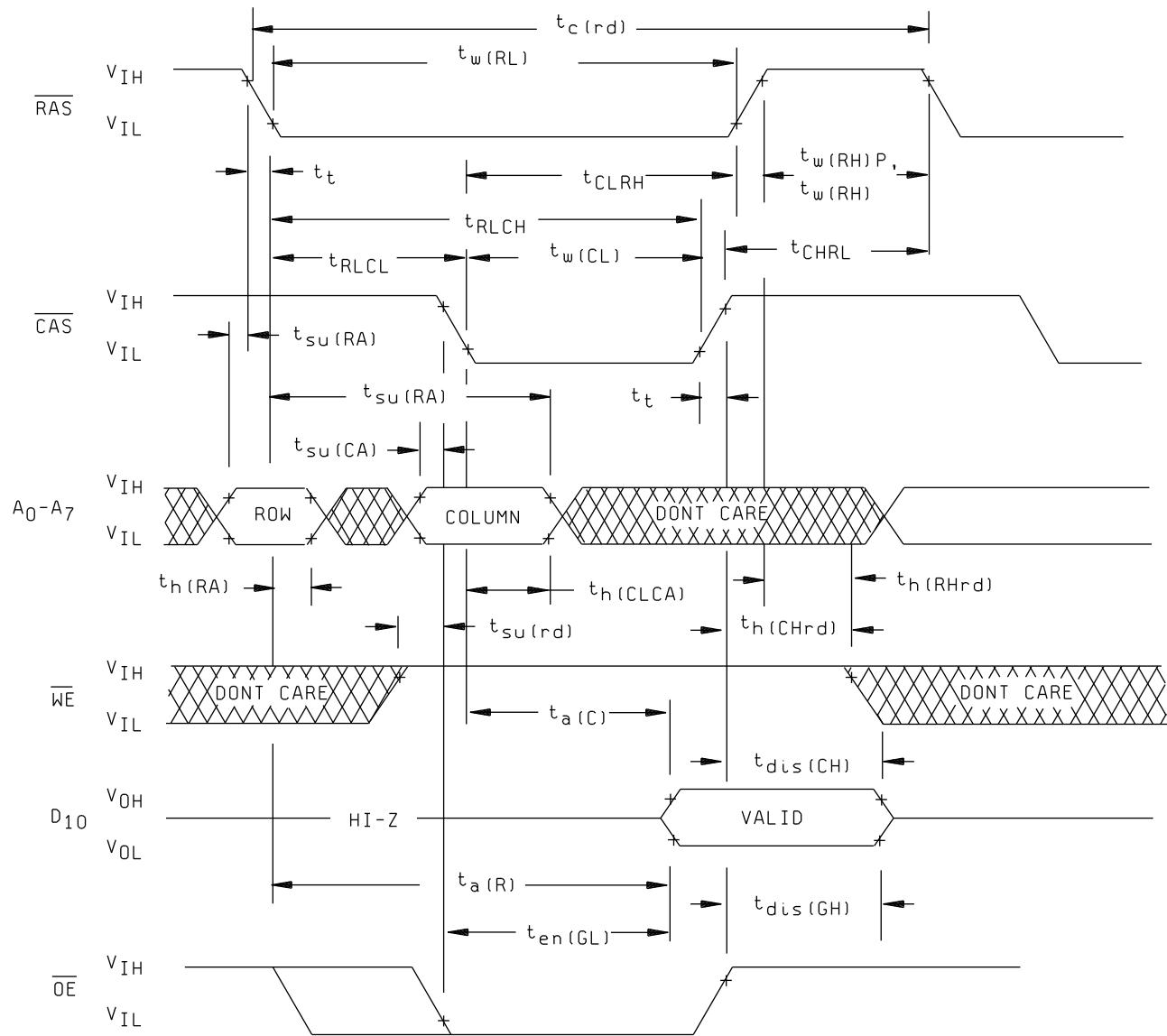


FIGURE 5. Switching waveforms - Continued.

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### Early write cycle

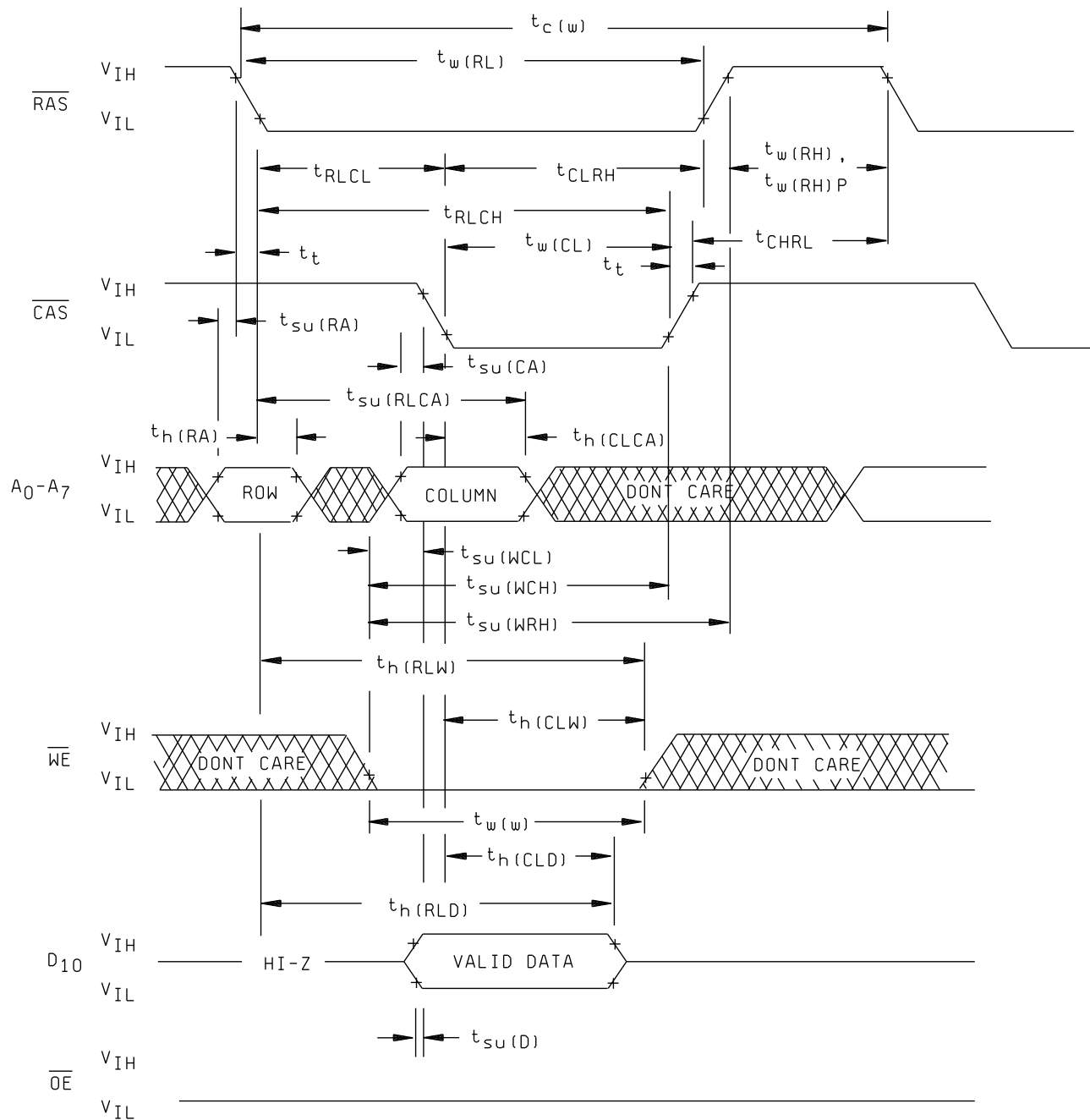


FIGURE 5. Switching waveforms - Continued.

# Read-write/read-modify-write cycle

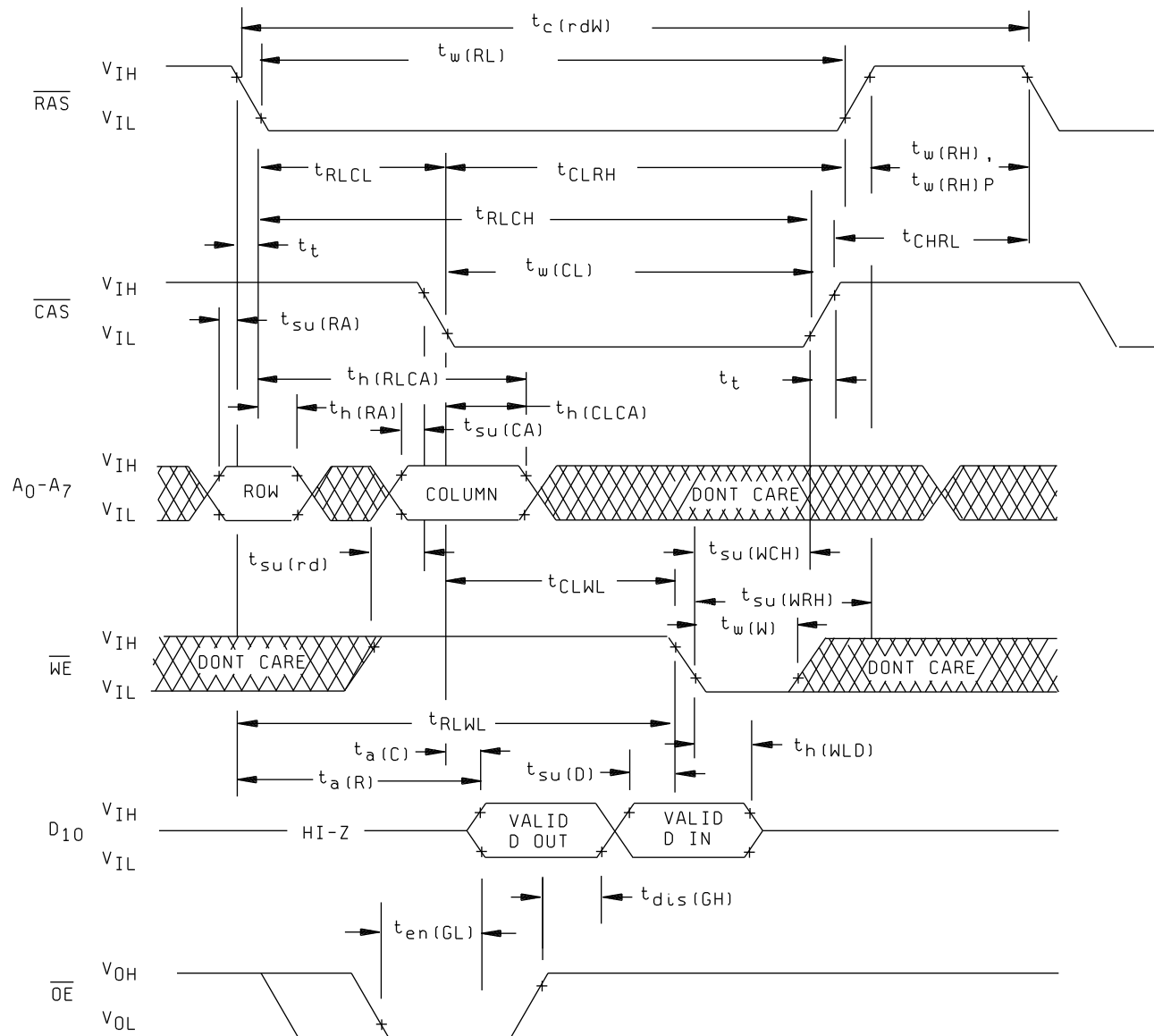


FIGURE 5. Switching waveforms - Continued.

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# Page-mode read cycle

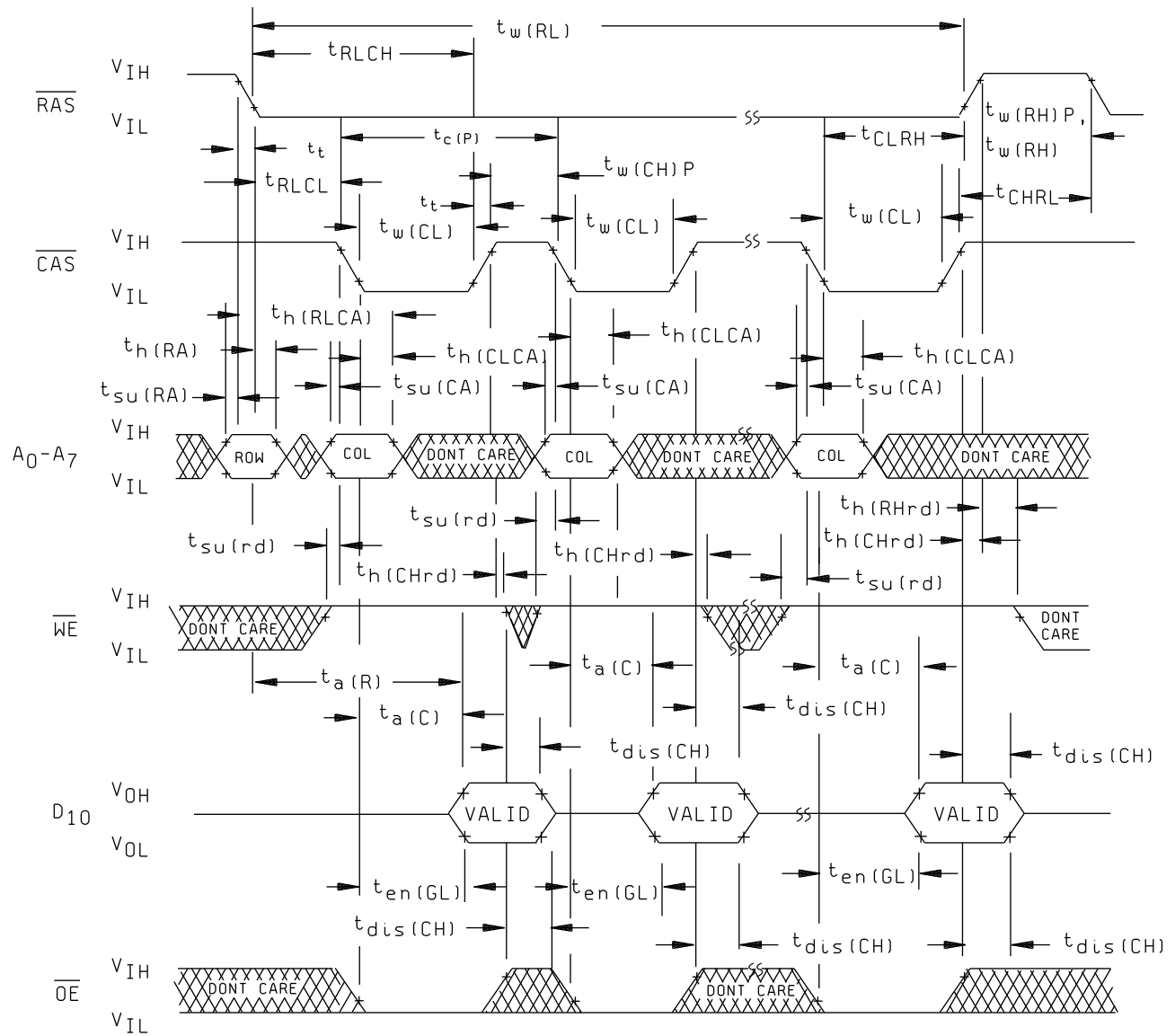


FIGURE 5. Switching waveforms - Continued.

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Page-mode early write cycle

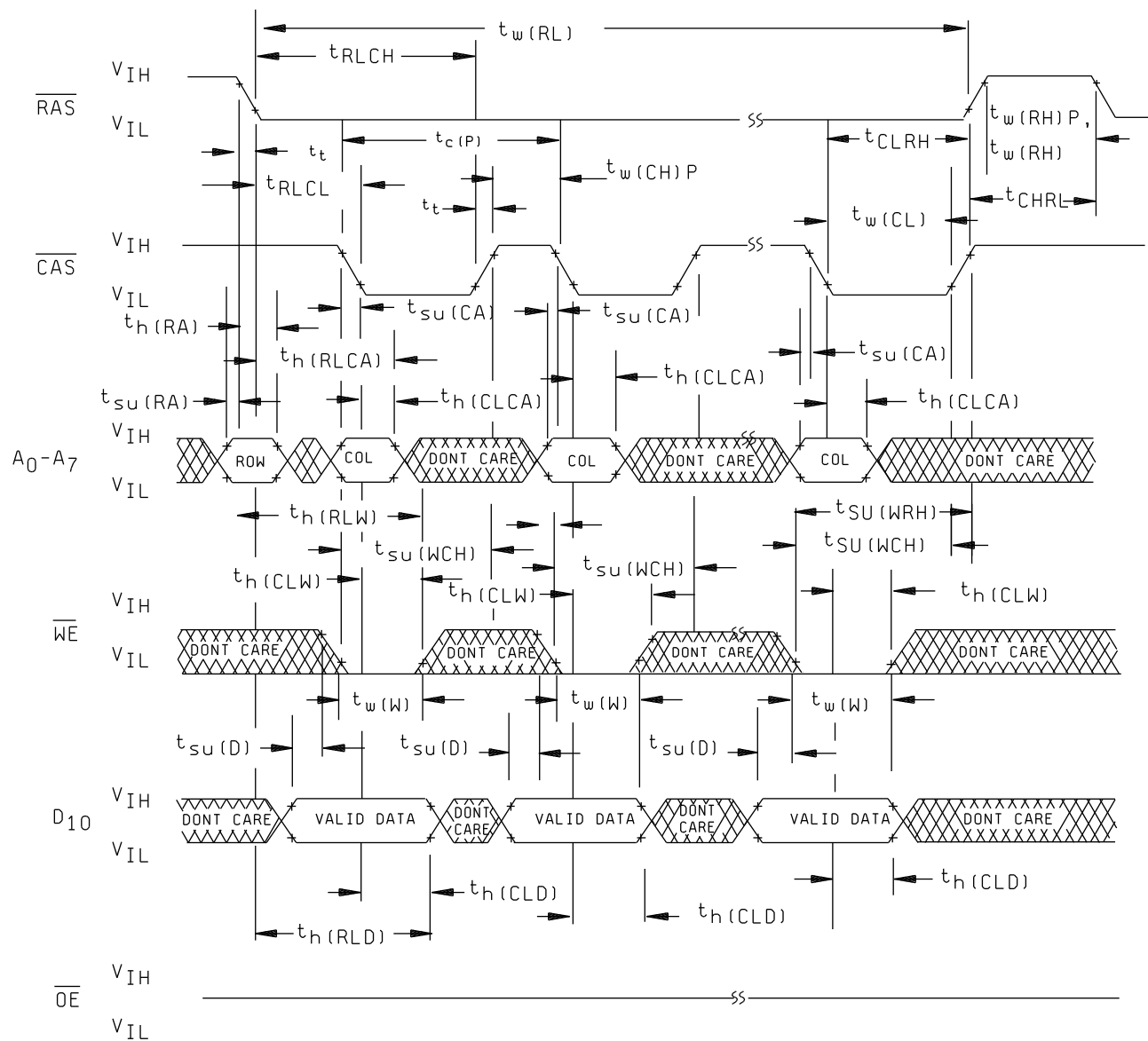


FIGURE 5. Switching waveforms - Continued.

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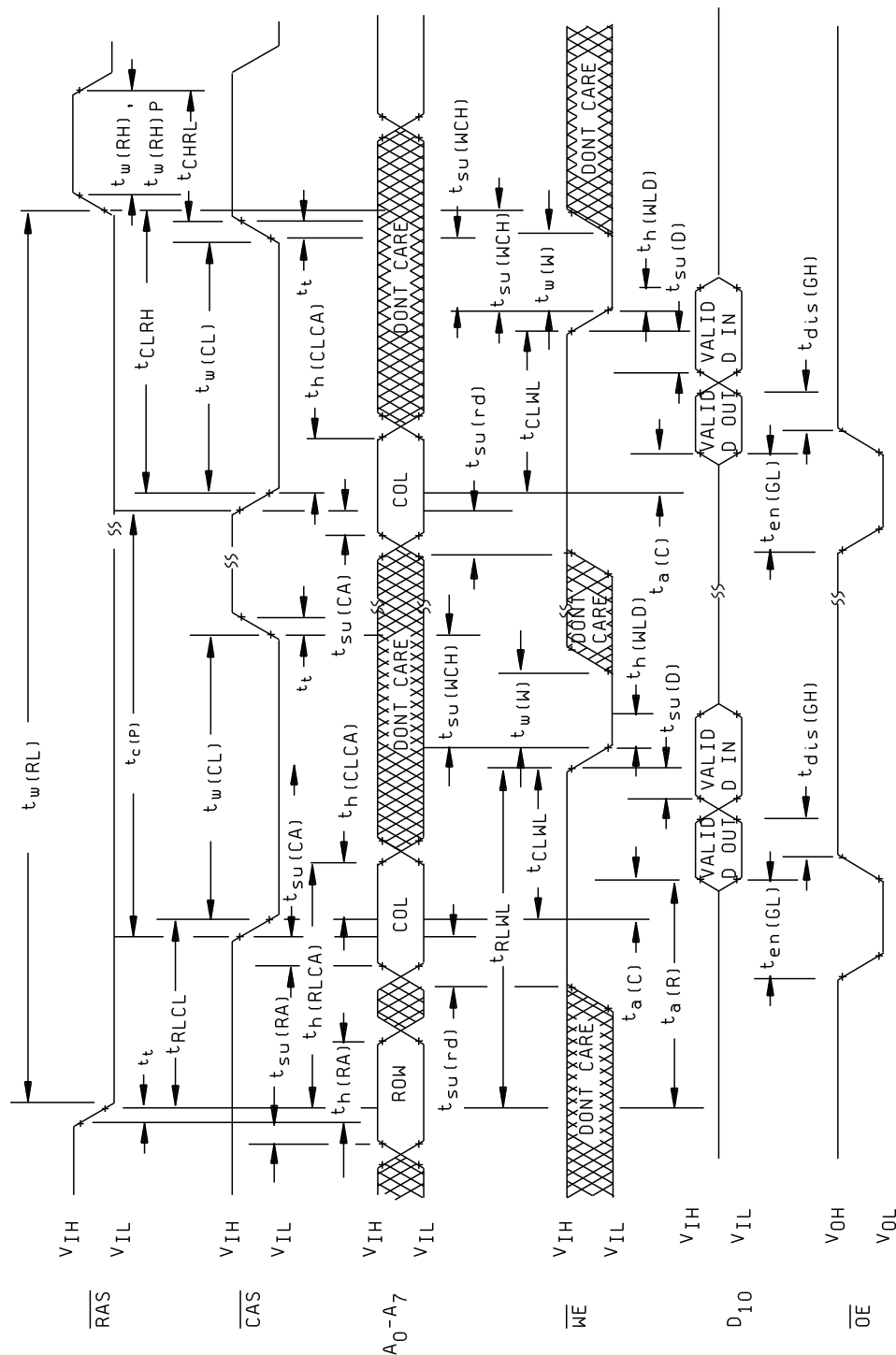


FIGURE 5. Switching waveforms - Continued.

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RAS-only refresh cycle

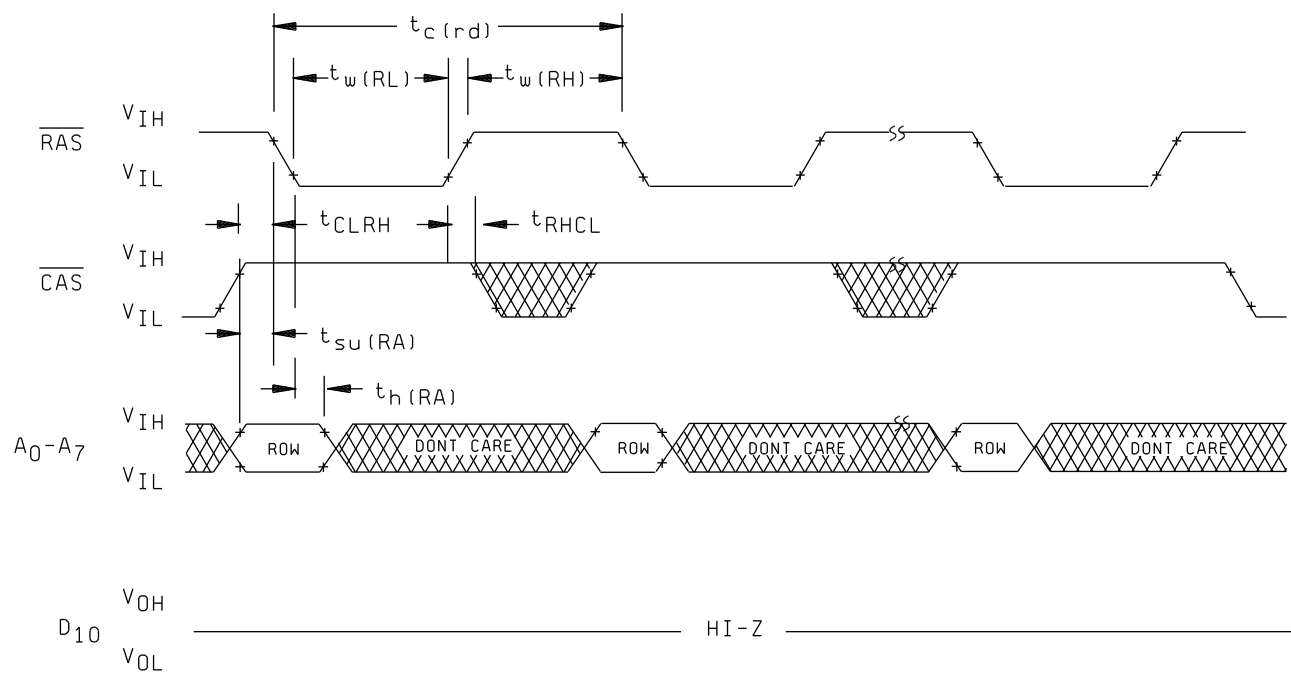


FIGURE 5. Switching waveforms - Continued.

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# Hidden refresh cycle

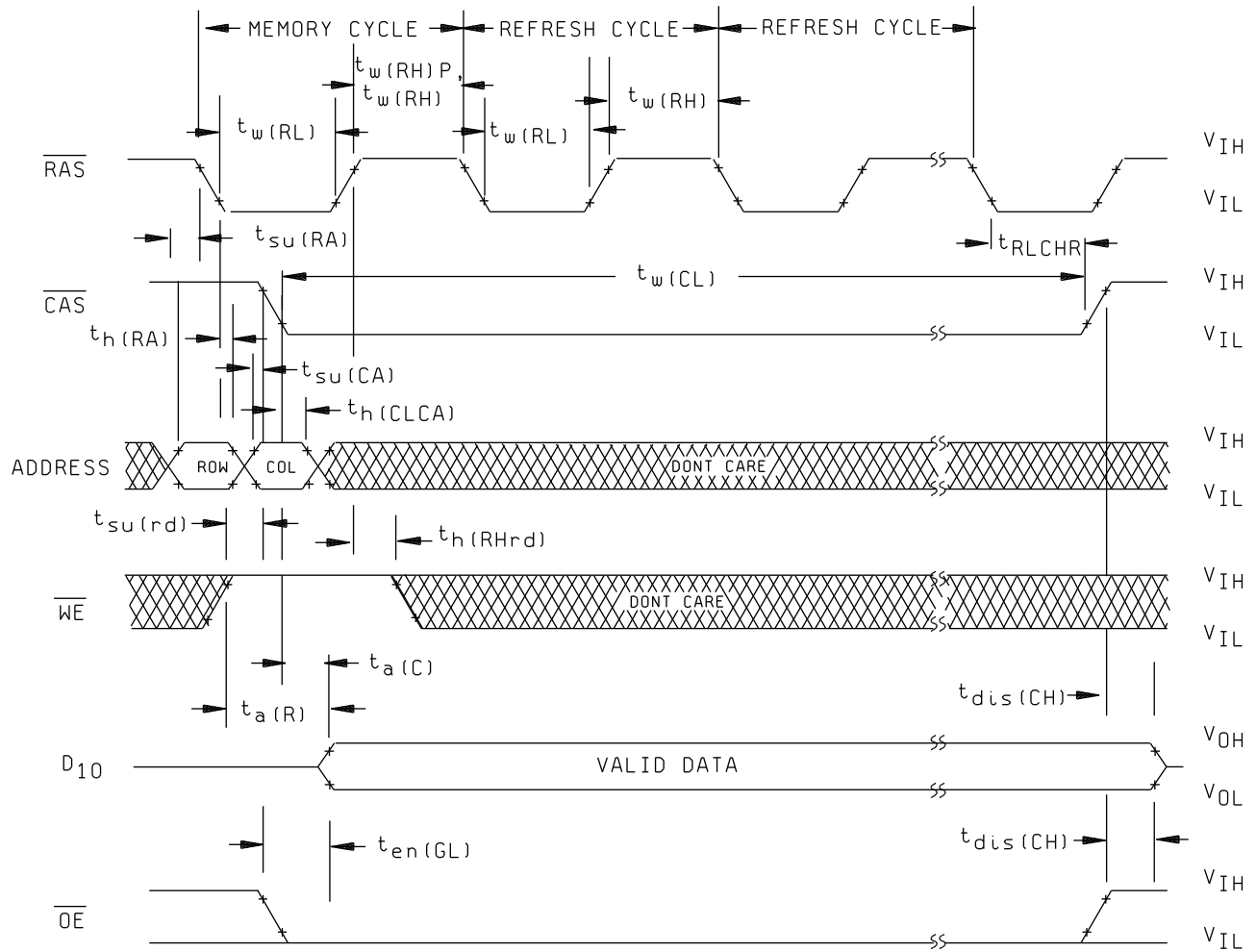


FIGURE 5. Switching waveforms - Continued.

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#### 4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

#### 4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.
- e. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

#### 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B Δ	2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ \* indicates PDA applies to subgroup 1 and 7.

5/ \*\* see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

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TABLE IIB. Delta limits at +25° C.

Parameter <sup>1/</sup>	Device types
	All
I <sub>CC3</sub> standby	±10% of specified value in table I
I <sub>IH</sub> , I <sub>IL</sub> , I <sub>OL</sub> , I <sub>OH</sub>	±10% of specified value in table I

<sup>1/</sup> The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T<sub>A</sub> = +25° C ±5° C, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.



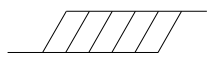

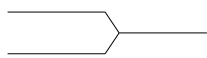
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6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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## APPENDIX

### FUNCTIONAL ALGORITHMS

#### 10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

#### 30. ALGORITHMS

##### 30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance ( $t_{OFF}$ ). This pattern verifies the output buffer switches to high impedance (three-state) within the specified  $t_{OFF}$  after the rise of CAS. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load address location with data.
- Step 3: Raise CAS and read address location and guarantee  $V_{OL} < V_{OUT} < V_{OH}$  after  $t_{OFF}$  delay.

##### 30.2 Algorithm B (pattern 2).

30.2.1  $V_{CC}$  slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data with  $V_{CC}$  at 5.0 V.
- Step 3: Change  $V_{CC}$  to 5.5 V.
- Step 4: Read memory with background data.
- Step 5: Load memory with background data complement.
- Step 6: Change  $V_{CC}$  to 4.5 V.
- Step 7: Read memory with background data complement.

##### 30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data.
- Step 3: Read location 0.
- Step 4: Write data complement in location 0.
- Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
- Step 6: Read data complement in maximum address location.
- Step 7: Write data in maximum address location.
- Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
- Step 9: Read data in maximum address location.
- Step 10: Write data complement in maximum address location.
- Step 11: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
- Step 12: Read memory with data complement.

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## APPENDIX - Continued

### 30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data.
- Step 3: Pause  $t_{REF}$  (stop all clocks).
- Step 4: Read memory with background data.
- Step 5: Repeat steps 2 through 4 with data complement.

### 30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data.
- Step 3: Read memory with data and load with data complement using RMW cycle.
- Step 4: Repeat step 3 for all address locations.
- Step 5: Repeat steps 2 and 3 using data complement.

### 30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load first page of memory with background data using Page mode cycle.
- Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
- Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
- Step 5: Repeat steps 2 through 4 for remaining memory locations.

### 30.7 Algorithm G (pattern 7).

30.7.1 CAS-before-RAS refresh test. This test is used to verify the functionality of the CAS before RAS mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data.
- Step 3: Perform 1024 CAS-before-RAS cycles while attempting to modify data.
- Step 4: Read memory with background data.

### 30.8 Algorithm H (pattern 8).

30.8.1 RAS-only refresh test. This test is used to verify the functionality of the RAS-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

- Step 1: Perform 8 pump cycles.
- Step 2: Load memory with background data.
- Step 3: Perform 1024 RAS-only cycles while attempting to modify data.
- Step 4: Repeat step 3 for 1 second.
- Step 5: Read memory with background data.

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## STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-09-06

Approved sources of supply for SMD 5962-92132 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-9213201MVX	0EU86	MT4C4067C-10 883C
5962-9213201MXX	0EU86	MT4C4067EC-10 883C
5962-9213201MYX	0EU86	MT4C4067EA-10 883C
5962-9213202MVX	0EU86	MT4C4067C-12 883C
5962-9213202MXX	0EU86	MT4C4067EC-12 883C
5962-9213202MYX	0EU86	MT4C4067EA-12 883C
5962-9213203MVX	0EU86	MT4C4067C-15 883C
5962-9213203MXX	0EU86	MT4C4067EC-15 883C
5962-9213203MYX	0EU86	MT4C4067EA-15 883C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

0EU86

Vendor name  
and address

Austin Semiconductor  
8701 Cross Park Drive  
Austin, TX 78754

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